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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,757	01/30/2004	Daisuke Yoshida	16869N-104300US	7064

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EXAMINER	
ANYIKIRE, CHIKAODILI E	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/768,757	YOSHIDA ET AL.	
	Examiner	Art Unit	
	CHIKAODILI E. ANYIKIRE	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application is responsive to application number (10768757) filed on January 30, 2004. Claims 1-14 are pending and have been examined.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 9, 2009 has been entered.

Response to Arguments

3. Applicant's arguments filed March 9, 2009 have been fully considered but they are not persuasive. The examiner understand the applicant's argument being that "the second bit rate of the first image signal being set higher than the first bit rate of the subset of image signal" (page 7 lines 7-8). The examiner respectfully disagrees due MacInnis by way of obviousness shows that the rate would be higher the than the decoding rate (the first rate).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al (US 2002/0106024) in view of MacInnis et al (US 2003/0215018).

As per **claim 1**, Sato et al disclose a signal processor which inputs a first image signal encoded by a first compressing and encoding method is inputted and in which the first image signal is transcoded to a second image signal encoded by a second compressing and encoding method, the signal processor comprising:

a picture selector (Fig 1, element 11) which generates a subset image signal of the first image signal by extracting pictures of one or more specific types in frames or fields from the first image signal (paragraph [0099]; Sato discloses a picture discrimination unit that extract I/P frames, discards the B frames);

a first decoder (Fig 1, element 13) which decodes the subset image signal generated by the picture selector at a decoding rate (paragraph [0103]; Sato discloses using a MPEG2 standard decoding unit to decode the extracted pictures); and

a first encoder (Fig 1, element 16), which encodes the decoded image signal by a second compressing and encoding method (paragraph [0105] Ln 7-12 and [0106]; Sato discloses using a MPEG4 standard encoded unit to encode the decoded frames);

a video stream supplying section configured to supply a bit rate of the first image signal to the picture selector (paragraph [0099]; Sato discloses sending an MPEG2 image to the picture selector (Fig 1 element 11) of the invention);

wherein the picture selector (Fig 1 element 11) uses the extracted pictures to generate the subset image signal whose effective length is reduced (paragraph [0099]; Sato discloses discarding B frames, therefore the subset image has a reduced effective length), and supplies the subset image signal at a first bit rate to the first decoder, the first bit rate of the subset image signal being set to correspond to the decoding rate of the subset image signal by the first decoder (paragraph [0100]; Sato discloses a code amount, bit rate, which leads to the decoding unit and therefore corresponds to the decoding rate); and

the video stream supplying section supplies the first image signal at second bit rate to the picture selector to compensate for an amount of code of the pictures which are not extracted by the picture selector (paragraph [0099] Ln 1-4; Sato discloses sending an MPEG2 image to the picture selector (Fig 1 element 11) of the invention and

sending the complete signal would therefore leave a bit rate that corresponds and compensates the picture selection time.

However, Sato et al does not explicitly teach the bit rate of the image signal being set higher than the decoding rate of the first decoder.

In the same field of endeavor, MacInnis et al teach the bit rate of the image signal being set higher than the decoding rate of the first decoder (paragraph [0037]).

Therefore, it would have been obvious for one having skill in the art at the time of the invention to modify the invention of Sato et al with the invention of MacInnis et al. The advantage is to provide a format less complex to decode.

Regarding **claim 2**, arguments analogous to those presented for claim 1 are applicable for claim 2.

As per **claim 3**, Sato et al disclose a signal processor according to claim 1, wherein the subset image signal has the extracted pictures arranged sequentially (Fig 3) therein and the effective length of the subset image signal is reduced (paragraph [0099] and [0104]).

As per **claim 4**, Sato et al disclose a signal processor according to claim 2, wherein the interface section extracts and reads out pictures of one or more specific types by referring to management information (paragraph [0100]; the prior art discloses information that is used to carry out the transcoding method) recorded along with the first image signal on the recording medium (paragraph [0099] and [0100]).

As per **claim 5**, Sato et al disclose a signal processor according to claim 1, wherein the picture selector performs picture extraction in such a manner that each extracted picture can refer to another extracted picture for motion compensation (paragraph [0106] - [0108]).

As per **claim 6**, Sato et al disclose a signal processor according to claim 1, wherein:

the first compressing and encoding method is an MPEG2 method ([0099] and [0103]) and the second compressing and encoding method is an MPEG4 method (paragraph [0105] Ln 7-12 and [0106]); and

the picture selector (Fig 1, 11) generates the subset image signal by extracting I-pictures and P-pictures (paragraph [0099]).

7. Claims 7, 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al (US 2002/0106024) in view of MacInnis et al (US 2003/0215018) in further view of Okada (US 2002/0181588).

As per **claim 7**, Sato et al disclose a signal processor according to claim 1.

However, Sato et al does not explicitly teach wherein the picture selector allows the user to specify what types of pictures are to be extracted.

In the same field of endeavor, Okada teaches a main control unit 536, which is comprised of a control core circuit 10, a CPU and so forth, controls each part in an overall and supervised manner according to instructions from the user. The instructions

form the user are inputted via remote control light receiving unit 548, which receives signals from, for example, a remote controller. A media I/F circuit 550 reads multimedia data or programs from an IC card, MO, CD-ROM, and DVD-ROM or other record media, which are not shown here, into a main control unit 536.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the signal processor of Sato et al with the remote control of Okada. The advantage of the remote controller is that it provides the ability of a person to control the parameters of the signal processor.

As per **claim 9**, Sato et al disclose a signal processor according to claim 1, further comprising:

a frame memory (Fig 1, 15) for storing the image signal decoded by the first decoder ([0106] Ln 1-2).

However, Sato et al does not explicitly teach a display section which reads out the image signal from the frame memory and outputs the image signal to a display unit;

wherein images being transcoded are displayed on the display unit.

In the same field of endeavor, Okada teaches the display circuit produces an image video signal from picture data transferred from the decoder 5 or the second decoder 7 and output this to the display 3 which is connected to the image reproducing apparatus 1 ([0062]).

The second decoder 7 reads out pictures included in recoded data sequences stored in the storage area 4a in the reverse time-series picture order, so as to be decoded. Thereby, a reproduced image data sequence is generated, and reverse reproduction is realized. This reproduced image data sequence is inputted to the display circuit 9 from the second node 8b of the switching circuit 8.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify the signal processor of Sato et al with the display of Okada. The advantage of the display of Okada is to provide visual imagery for the transcoded image data.

As per **claim 10**, Sato et al disclose an imaging apparatus using the signal processor according to claim 1 (as discussed in the rejection of claim 1).

However, Sato et al does not explicitly teach an image apparatus comprising:

an image pickup section which picks up an object;

a second encoder which, by the first compressing and encoding method, encodes the first image signal supplied from the image pickup section; and

a recording and reproducing section which records and reproduces the first image signal encoded by the second encoder to and from a recording medium,

wherein the first image signal reproduced from the recording medium is supplied to the signal processor.

In the same field of endeavor, as shown in Fig 3, Okada teaches a block circuit of an image reproducing apparatus 1 is incorporated into a movie camera, a still camera, a television, a video CD reproduction apparatus or a DVD reproduction apparatus, which outputs the MPEG video stream from a transfer medium 2 to a display 3.

Okada teaches an image pickup section which picks up an object ([0057] Ln 17-19; the prior art discloses a transfer medium to be an image pickup);

a second encoder which, by the first compressing and encoding method, encodes the first image signal supplied from the image pickup section ([0057] Ln 11-15); and

a recording and reproducing section which records and reproduces the first image signal encoded by the second encoder to and from a recording medium ([0057] Ln 3-11; [0058]),

wherein the first image signal reproduced from the recording medium is supplied to the signal processor ([0058] Ln 1-5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to integrate the signal processor of Sato et al with the image apparatus of Okada because it provides a transfer medium for the MPEG bitstream, capable of obtaining smooth reverse-reproduced pictures (Okada [0020]).

As per **claim 11**, Sato et al disclose a signal processor (as discussed in the rejection of claim 1).

However, Sato et al does not explicitly teach an imaging apparatus according to claim 10, further comprising:

a receiver which receives an image signal from the outside;

wherein the second encoder encodes the image signal supplied from the receiver by the first compressing and encoding method.

In the same field of endeavor, as shown in Fig 3 Okada teaches a block circuit of an image reproducing apparatus 1 is incorporated into a movie camera, a still camera, a television, a video CD reproduction apparatus or a DVD reproduction apparatus, which outputs the MPEG video stream from a transfer medium 2 to a display 3.

Okada teaches a receiver which receives an image signal from the outside (Fig 3, 1; [0057] Ln 1-7);

wherein the second encoder encodes the image signal supplied from the receiver by the first compressing and encoding method ([0057] Ln 11-15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to integrate the signal processor of Sato et al with the image apparatus of Okada because it provides a transfer medium for the MPEG bitstream, capable of obtaining smooth reverse-reproduced pictures (Okada [0020]).

As per **claim 12**, Sato et al disclose a signal processor (as discussed in the rejection of claim 1).

However, Sato et al does not explicitly teach an imaging apparatus according to claim 10, further comprising:

a receiver which receives the first image signal encoded by the first compressing and encoding method from the outside;

wherein the recording and reproducing section records and reproduces the first image signal supplied from the receiver to and from the recording medium.

In the same field of endeavor, as shown in Fig 3, Okada teaches a block circuit of an image reproducing apparatus 1 is incorporated into a movie camera, a still camera, a television, a video CD reproduction apparatus or a DVD reproduction apparatus, which outputs the MPEG video stream from a transfer medium 2 to a display 3.

Okada teaches a receiver which receives the first image signal encoded by the first compressing and encoding method from the outside (Fig 3, 1, [0057] Ln 7-14);

wherein the recording and reproducing section records and reproduces the first image signal supplied from the receiver to and from the recording medium. (Fig 3, 4, [0057] Ln 7-14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to integrate the signal processor of Sato et al with the image apparatus of Okada because it provides a transfer medium for the MPEG bitstream, capable of obtaining smooth reverse-reproduced pictures (Okada [0020]).

As per **claim 13**, Sato et al disclose a signal processor (as discussed in the rejection of claim 1).

However, Sato et al does not explicitly teaches an imaging apparatus according to claim 10, wherein the recording and reproducing apparatus generates management information from the first image signal recorded on the recording medium and records the management information on the recording medium.

In the same field of endeavor, Okada teaches Fig 3 shows a block circuit of an image reproducing apparatus 1 is incorporated into a movie camera, a still camera, a television, a video CD reproduction apparatus or a DVD reproduction apparatus, which outputs the MPEG video stream from a transfer medium 2 to a display 3.

Okada teaches wherein the recording and reproducing apparatus generates management information from the first image signal recorded on the recording medium and records the management information on the recording medium ([0057] Ln 3-15; the prior art discloses DVD and CD medium also the MPEG standard include management information in order to playback or decode a video stream).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to integrate the signal processor of Sato et al with the image apparatus of Okada. because it provides a transfer medium for the MPEG bitstream, capable of obtaining smooth reverse-reproduced pictures (Okada [0020]).

As per **claim 14**, Sato et al discloses a signal processor according to claim 1 (as discussed in the rejection of claim 1),

wherein it transcodes the first image signal to a second image signal encoded by a second compressing and encoding method and outputs the second image signal to external equipment ([0097]).

However, Sato et al does not explicitly teach a signal processor using the signal processor according to claim 1, wherein said signal processor inputs a first image signal encoded by a first compressing and encoding method.

In the same field of endeavor, as shown in Fig 3, Okada teaches a block circuit of an image reproducing apparatus 1 is incorporated into a movie camera, a still camera, a television, a video CD reproduction apparatus or a DVD reproduction apparatus, which outputs the MPEG video stream from a transfer medium 2 to a display 3.

Okada teaches wherein said signal processor inputs a first image signal encoded by a first compressing and encoding method ([0057] Ln 14-19).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to integrate the signal processor of Sato et al with the image apparatus of Okada because it provides a transfer medium for the MPEG bitstream, capable of obtaining smooth reverse-reproduced pictures (Okada [0020]).

Other Prior Art Cited

8. The following prior art are relevant art that can be applied to the application currently pending.

Masukura et al (US 2003/0001964) discloses a signal processor with a display and contains a processor parameter controller.

Haraguchi et al (US 2004/0218671) discloses a signal processor that decodes a MPEG2 signal and encodes a MPEG 4 encoder. It also contains a picture type decision block.

Ramakrishnan et al (US 7, 173, 947) discloses a signal processor that provides management information and rate controller.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHIKAODILI E. ANYIKIRE whose telephone number is (571)270-1445. The examiner can normally be reached on Monday to Friday, 7:30 am to 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272 - 7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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